Operation Cycles of DMAC

There are mainly two operation cycles of a DMAC.

I. **Idle Cycle**
- **After Reset**, the DMAC is in idle state (idle cycle).
- During idle state, **no DMA operation is taking place.**
- **No DMA requests** are **active.**
- The **initialization** of the DMAC takes place in the idle mode.

II. **Active Cycle**
- Once **DMA operation begins,** the **DMAC** is said to be **in active mode.**
- Now the **DMAC controls** the **system bus.**
- There are **three types of ACTIVE DMA Cycles** while performing DMA transfer:

1) **DMA Read**
- The DMAC **reads** data **from** the **memory** and **writes into** to the **I/O device.**
- Thus, **MEMR** and **IOW** signals are used.

2) **DMA Write**
- The DMAC **reads** data **from** the **I/O device** and **writes into** to the **memory.**
- Thus, **IOR** and **MEMW** signals are used.

3) **DMA Verify**
- In this cycle, 8237 does not generate any control signals. Hence, no data transfer takes place.
- During this time, the peripheral and the DMAC verify the correctness of the data transferred, using some error detection method.

Transfer Modes of 8237

8237 has **four modes of data transfer:**

1) Single Transfer Mode.
- In this mode, the DMAC is programmed to **transfer ONLY ONE BYTE** in one complete DMA operation.
- After a byte is transferred, the **CAR** and **CWCR are adjusted** accordingly.
- The **system bus is returned** to the **µP.**
- For further bytes to be transfegred, **the DREQ line must go active again,** and then the entire operation is repeated.

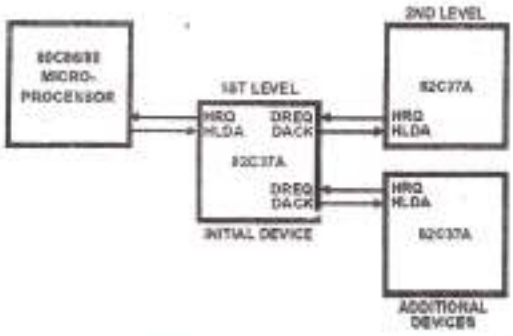
2) Block Transfer Mode.
- In this mode, the DMAC is programmed to **transfer ALL THE BYTES** in one complete DMA operation.
- After a byte is transferred, the **CAR and CWCR are adjusted** accordingly.
- The **system bus** is **returned** to the **µP, ONLY after all the bytes are transferred.** I.e. **TC** is **reached** or **EOP** signal is issued.
- The **DREQ** signal **needs to be active only in the beginning** for requesting the DMA service initially.
- Thereafter **DREQ** can **become low during the transfer.**

3) Demand Transfer Mode.

- It is very **similar to Block Transfer**, **except** that the **DREQ must active throughout the DMA operation.**
- **If** during the operation **DREQ goes low**, the **DMA operation is stopped** and the **busses** are **returned** to the **µP.**
- In the meantime, the **µP** can **continue** with its own operations.
- **Once DREQ goes high again**, the **DMA operation continues** from where it had stopped.

4) Cascade Transfer Mode.

- In this mode, **more than one DMACs** are cascaded together.
- It is used to **increase** the **number of devices interfaced** to the **µP.**
- Here we have **one Master DMAC**, to which **one or more Slave DMACs** are connected.
- The **Slave gives HRQ** to the Master **on the DREQ of the Master**, and the **Master gives HRQ** to the **µP on the HOLD of the µP.**



Priority Methods of 8237

8237 has **two priority methods:**

1) Fixed Priority.

- This is the **default** mode of 8237.
- Here the priorities of the channels are fixed.
- **Channel 0 has the highest priority**, followed by Channel 1, Channel 2 and finally **Channel 3** having the lowest **priority.**

2) Rotating Priority.

- It is a **flexible** priority mode.
- In this mode, the Channel, which was **most recently serviced, receives the lowest priority.**
- This **prevents** any **one Channel from dominating** the system.